ABSTRACT OF THE DISCLOSURE

A shift-register unit. The first transistor includes a first source/drain coupled to a first terminal, a second source/drain, and a first gate coupled to a reset signal to stop the shift-register unit outputting a pulse signal. The second transistor includes a third source/drain coupled to the second source/drain, a fourth source/drain coupled to a second terminal, and a second gate coupled to a setting signal to initial the shift-register unit. The third transistor includes a fifth source/drain coupled to an output terminal, a third gate coupled to the second source/drain and a sixth source/drain coupled to a clock signal to start outputting the pulse signal. The fourth transistor includes a seventh source/drain coupled to the first terminal, an eighth source/drain coupled to the output terminal and a fourth gate coupled to a refresh signal to set a voltage level of the shift-register unit in a standby mode.